

Claims 23-26 are cancelled.

sub 01  
C1

27. (Amended) A gate stack, comprising:  
a polysilicon layer over a semiconductive substrate;  
a gate oxide layer on the polysilicon layer;  
a metal silicide layer on the gate oxide layer;  
a layer comprising  $\text{Si}_x\text{N}_y\text{O}_z\text{:H}$  over and in physical contact with the metal silicide,  
wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33; and  
a silicon nitride layer on the layer comprising  $\text{Si}_x\text{N}_y\text{O}_z\text{:H}$ .

Claims 28-32 are cancelled.

C2 sub 01

33. (Amended) The gate stack of Claim 27, where the layer comprising  $\text{Si}_x\text{N}_y\text{O}_z\text{:H}$  has a thickness of from about 250Å to about 650Å.

Claims 34-35 are cancelled.

sub 01  
C3

36. (New) The gate stack of claim 27 wherein y is from 0.02 to less than 0.1.

37. (New) The gate stack of claim 27 wherein x=0.5, y=0.37 and z=0.13.